I) IN THE CLAIMS

1. (Original) A noise filter for an integrated circuit comprising:

a CMOS inverter having an input and an output, said input of said CMOS inverter being coupled with an input pad of said integrated circuit, said output of said CMOS inverter being coupled with an input buffer;

a first capacitor being inserted between said output of said CMOS inverter and a first voltage source; and

a second capacitor being inserted between said output of said CMOS inverter and a second voltage source.

2. (Original) A noise filter according to Claim 1, wherein said integrated circuit is an LSI.

3. (Original) A noise filter according to Claim 1, wherein said integrated circuit is a VLSI.

4. (Original) A noise filter according to Claim 1, wherein said input buffer is a schmitt trigger.

5. (Original) A noise filter according to Claim 1, wherein said CMOS inverter includes a NMOS transistor and a PMOS transistor.

6. (Original) A noise filter according to Claim 1, wherein said first voltage source is VDD and said second voltage source is VSS.

7. (Amended) A noise filter for an integrated circuit comprising:

a transition circuit having an input and an output, said input of said transition circuit being coupled with an input pad of said integrated circuit, said output of said transition circuit being coupled with an input buffer;

a first capacitor being inserted between said output of said transition circuit and a first voltage source; and

a second capacitor being inserted between said output of said transition circuit and a second voltage source;

said transition circuit comprising with a Pch MOS transistor and a Nch MOS transistor;

the source of said Pch MOS transistor and the Nch MOS transistor being coupled with the input of said transition circuit;

the drain of said Pch MOS transistor and the Nch MOS transistor being coupled with the output of said transition circuit;

the gate of said Pch MOS transistor being coupled with a first reference voltage;

the gate of said Nch MOS transistor being coupled with a second reference voltage.

8. (Original) A noise filter according to Claim 7, wherein said integrated circuit is an LSI.

9. (Original) A noise filter according to Claim 7, wherein said integrated circuit is a VLSI.

10. (Original) A noise filter according to Claim 7, wherein said transition circuit includes two transfer gates, the two transfer gates are a NMOS transistor and a PMOS transistor.

11. (Original) A noise filter according to Claim 7, wherein said input buffer is a schmitt trigger.

12. (Original) A noise filter according to Claim 7, wherein said first voltage source is VDD.

13. (Original) A noise filter according to Claim 12, wherein a reference voltage of said transition circuit is VDD/2.

14. (Original) A noise filter according to Claim 12, wherein said second voltage source is VSS.